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MHKKG/SUN P.O. BOX 398 AUSTIN, TX 78767			EXAMINER HUSSAIN, TAUQIR	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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## **DETAILED ACTION**

### ***Response to Amendment***

1. This office action is in response to amendment /reconsideration filed on 06/30/2009, the amendment/reconsideration has been considered. Claims 69, 82, 86, 89 and 90 have been amended, claims 74, 75, 91, 92, 98 and 99 have been canceled, claim 104 has been newly added and therefore, claims 69-73, 76-82, 86-90, 93-97 and 100-104 are pending for examination, the rejection cited as stated below.

### ***Response to Arguments***

2. Applicant's arguments have been fully considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 69-73, 76-80, 82, 86-90, 93-97, 100 and 104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwartz et al (Pub. No.: US 2005/0071625 A1), hereinafter "Schwartz" in view of Garg et al (Pub No: 2005/0193229 A1), hereinafter "Garg".

5. As to claim 69, 82, 86 and 104, Schwartz discloses,  
a switch portion (Schwartz, Fig.2, element-222);  
a service processor portion (Schwartz, Fig.2, element-214);

a data interface configured to communicate with an external management entity via a network (Fig.2, element-218 connected to remote manager 220);

Schwartz however is silent on disclosing explicitly, a fault management unit configured to receive fault messages generated by the switch portion and by the service processor portion including respective fault messages generated by the switch portion and the service processor portion that relate to a common fault, and wherein the fault management unit is further configured to perform processing on a received fault message to determine whether to forward the received message to the external management entity via the data interface, wherein the fault management unit is configured to not forward fault messages that relate to a fault for which the fault management unit has already forwarded a fault message to the external management entity.

Garg however discloses a similar architecture of fault tolerant system as the claim invention where, a fault management unit configured to receive fault messages generated by the switch portion and by the service processor portion including respective fault messages generated by the switch portion and the service processor portion that relate to a common fault (Garg, Fig.17, element- Fault Manager, [0046], The System Controller achieves this by activating the standby of all the failed resource sets in fault-tolerant configurations, or by reassigning and activating failed resource sets on to the available active processors in pure distributed configurations. Depending on the processor availability, the System Controller may also recreate affected standbys on the remaining available processors. The same procedure can be used to recover from

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multiple failures) and wherein the fault management unit is further configured to perform processing on a received fault message to determine whether to forward the received message to the external management entity via the data interface, wherein the fault management unit is configured to not forward fault messages that relate to a fault for which the fault management unit has already forwarded a fault message to the external management entity (Garg, [0405], If any of the above-mentioned steps of the scForcedSwitchover( ) command fail to complete successfully, the System Controller generates an alarm indicating the failure. The Fault Manager module uses this alarm to identify the location and cause of the failure. The Fault Manager isolates the new failure and typically issues a new scForcedSwitchover( ) command to the System Controller to recover from the new failure).

Therefore, it would have been obvious to one of the ordinary skilled in the art at the time the invention was made to combine the teachings of Schwartz with the teaching of Garg in order to provide a an Application Distributed Fault-Tolerant-High Availability Support Module (ADSM) to handle the resource set abstraction within the application. The ADSM is combined with the application only when the application has to operate in distributed or fault-tolerant configuration. ADSM and the application are placed together on every processor in which the application has to be operated in fault-tolerant or distributed mode. The ADSM is specific to each application and uses the warm standby approach for fault-tolerance.

6. As to claim 70, 87 and 94, Schwartz and Garg discloses the invention substantially as in parent claim 69, 82 and 86 above, including, wherein the fault

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management unit is implemented within the service processor portion (Schwartz, Fig.2, element-214 and 210, where service processor and scalability management modules are within same entity).

7. As to claim 71,88 and 95, Schwartz and Garg discloses the invention substantially as in parent claim 69, 82 and 86 above, including, wherein the fault management unit stores details of fault messages received irrespective of whether the message is forwarded to the external management entity (Garg, [0336], On receiving this command, the application allocates required resources to process and store state information of the resource sets as specified in update messages received from the active counterpart.).

8. As to claim 72, 89 and 96 Schwartz and Garg discloses the invention substantially as in parent claim 69, 82 and 86 above, including, wherein the stored details of the fault messages includes data describing an action taken by the originator of the fault message in response to detection of the fault (Garg, [0332], The return value of this function indicates whether all the resource sets of the application could be made standby successfully on the specified processor. If the return value indicates failure, none of the specified resource sets of any of the specified applications will be made standby. If the return value indicates success, all resource sets of all specified applications have been made standby successfully.).

9. As to claim 73, 90 and 97, carries similar limitations as claims 72, 89 and 96 and therefore are rejected under for same rationale.

10. As to claim 76, Schwartz and Garg discloses the invention substantially as in parent claim 69 above, including, wherein the switch portion and service processor portion are implemented by separate hardware within the module (Schwartz, Fig.2, Elements- 222 a switch and 214, a service processor are separate hardware).

11. As to claim 77, Schwartz and Garg discloses the invention substantially as in parent claim 69 above, including, wherein the switch portion and service processor portion are implemented by common hardware within the module (Schwartz, element-200, where switch portion and service processor portion are implemented by common hardware).

12. As to claim 78, 93 and 100, Schwartz and Garg discloses the invention substantially as in parent claim 69 above, including, wherein the service processor portion is configured to operate in master/slave relationship with a service processor portion of a further combined switch and service processor module of the modular computer system (Schwartz, [0018], where four RXE-216 are coupled to SMM-212 which is controlled via master scalability chipset 210 and since RXE-216 is remote and therefore is equivalent to slave entity); and

Wherein the service processor portion is further configured to automatically synchronize management information with the service processor portion of the further combined switch and service processor via the data interface in accordance with the master/slave relationship (Schwartz, Fig.3, element-312, [0019], where registering node with scalability manager module is synchronizing master/slave relationship).

13. As to claim 79, carry similar limitations as claim 69 and 78 above and therefore is rejected under for same rationale.

14. As to claim 80, The combined switch and service processor module of claim 69, wherein the service processor portion has a user interface configured to receive and forward communications between the external management entity and the switch portion (Schwartz, Fig.2, element-200, where SMM is the interface to control messages).

15. Claim 81 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schwartz and Garg in view of Ohkubo et al (Patent Number: US 5276683), hereinafter "Ohkubo".

16. As to claim 81, Schwartz and Garg disclose the invention substantially as in parent claims 69 above, including, wherein the switch and service processor elements are each operable to create a unique identifier using data unique to the respective processor (Schwartz, Fig.2, element-212, [0020], where SMM is available to the booting node and compares the stored UUID list to the nodes specific UUID); and

Schwartz however is silent on disclosing explicitly, wherein the service processor is operable to supply its unique identifier to the switch for use by the switch in identifying itself in precedence to the switch's own unique identifier.

Ohkubo however discloses the concept of aliasing or creating single ID for multiple or plurality of devices, wherein the service processor is operable to supply its



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unique identifier to the switch for use by the switch in identifying itself in precedence to the switch's own unique identifier (Ohkubo, Abstract, where masking circuit is used to select a plurality of instruments by using a single ID code).

Therefore, it would have been obvious to one of the ordinary skilled in the art at the time the invention was made to combine the teachings of Schwartz and Garg with the teachings of Ohkubo in order to provide a multiplex communication system having a received ID comparison system capable of effecting the high-speed data transfer with a small number of hardware.

17. Claims 101,102 and 103 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwartz and Garg in view of Tzeng et al (Pub. No.: US 2005/0122825 A1), hereinafter "Tzeng".

18. As to claim 101,102 and 103, Schwartz and Harper discloses the invention substantially as in parent claim 69, 82 and 86 above, including, detect a fault in an information processing module coupled to the switch portion (Garg, Abstract, The architecture also allows for a Fault Manager, which performs fault detection, fault location, and fault isolation, and uses the System Controller's API to initiate fault recovery.);

convey a corresponding fault message to the fault management unit (Garg, [0046], Another advantage of the invention is to allow the application to recover from multiple failures and redistribute incoming traffic on failures. The System Controller achieves this by activating the standby of all the failed resource sets in fault-tolerant

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configurations, or by reassigning and activating failed resource sets on to the available active processors in pure distributed configurations.).

Schwartz and Garg however are silent on disclosing explicitly, in response to detecting a fault in the information processing module: disable the network port of the information processing module.

Tzeng however discloses a similar concept of, in response to detecting a fault in the information processing module: disable the network port of the information processing module (Tzeng, [0351], where after receiving a warning message port is disabled or traffic is stopped from the said port).

Therefore, it would have been obvious to one of the ordinary skilled in the art at the time the invention was made to combine the teachings of Schwartz and Garg with the teachings of Tzeng in order to provide a high performance network switching architecture for integrating multiple switched into a single device and more control over port management.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TAUQIR HUSSAIN whose telephone number is (571)270-1247. The examiner can normally be reached on 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thu Nguyen can be reached on 571 272 6967. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. H./  
Examiner, Art Unit 2452

/Kenny S Lin/  
Primary Examiner, Art Unit 2452